ABSTRACT OF THE DISCLOSURE

In a method of testing a multi-port memory in accordance with a test pattern, test clock signals having the same test clock frequency but with different delay periods introduced therein are generated for controlling memory access through the different access ports of the memory. Consecutive memory operations of a test element of the test pattern are then conducted in a folded sequence upon a memory cell through the different access ports in accordance with the test clock signals such that the memory operations are completed within the same test clock cycle of the test element.